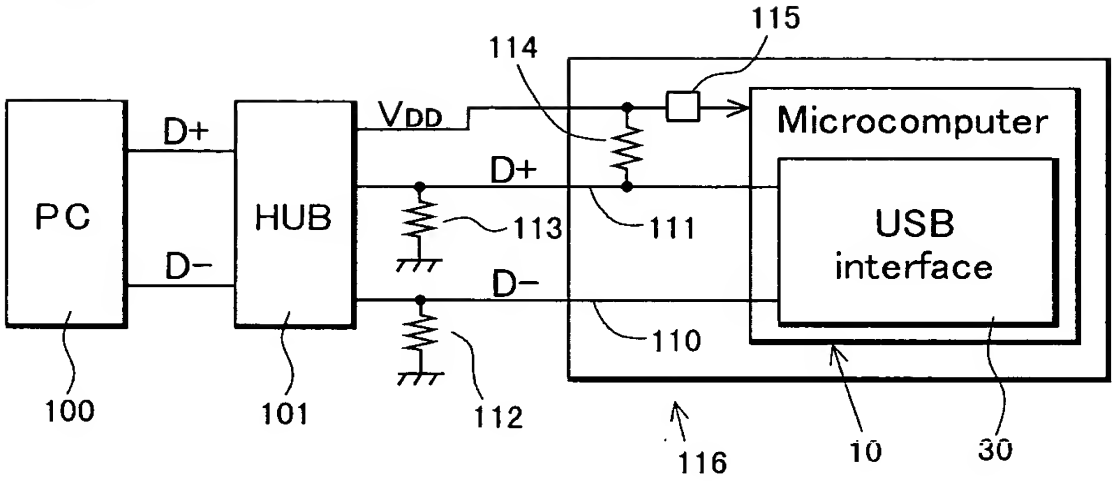
Fig.1


115
114
Microcomputer
PC
D+
HUB
VDD
D+
USB
interface
113
111
D-
D-
110
100
101
112
116
10
30

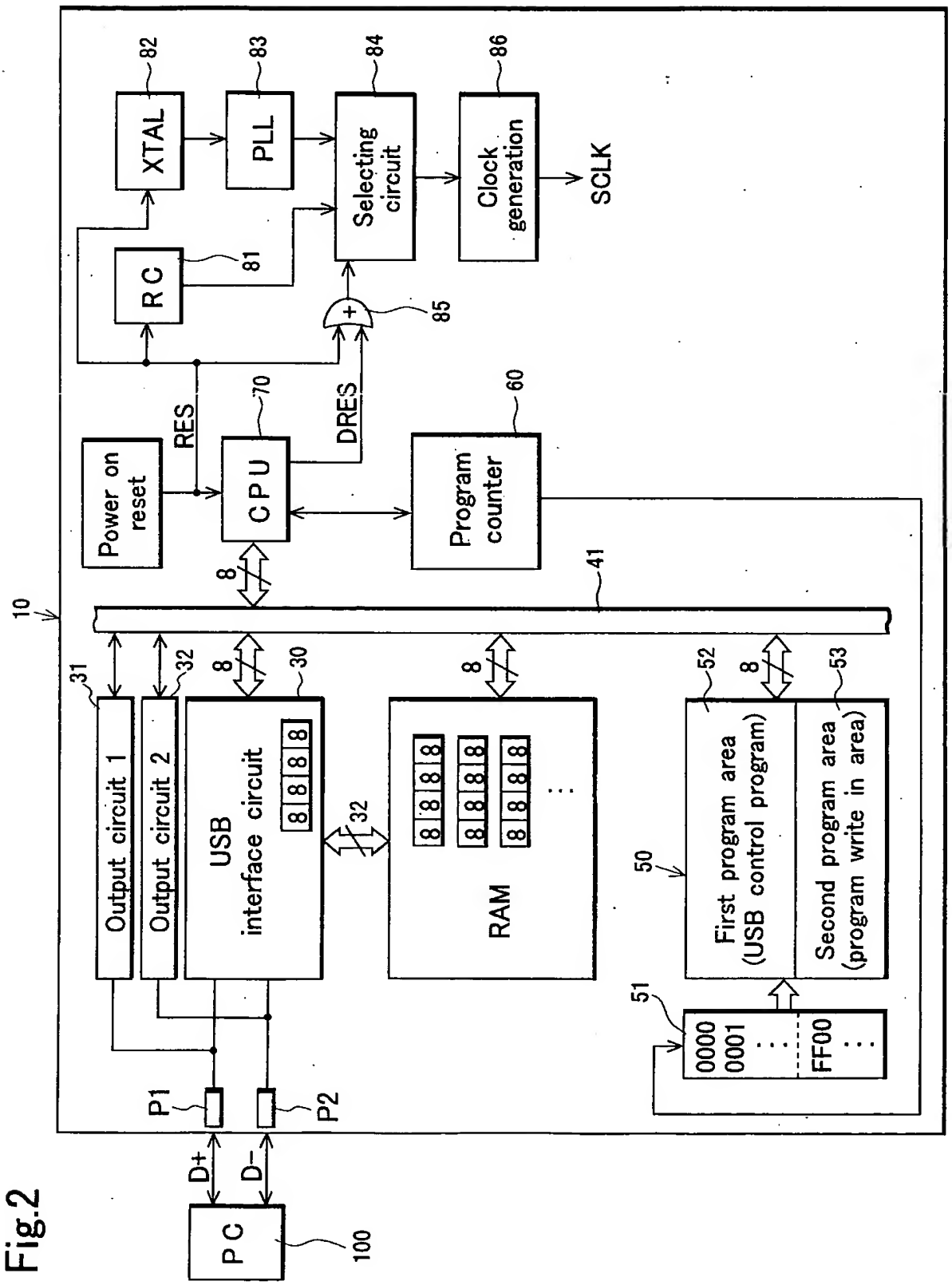

10
XTAL
82
PLL
83
Selecting circuit
84
Clock generation
86
SCLK
RC
81
85
+
RES
DRES
Power on reset
CPU
70
Program counter
60
8
41
31
32
30
Output circuit 1
Output circuit 2
USB interface circuit
RAM
50
52
53
First program area (USB control program)
Second program area (program write in area)
51
0000
0001
FF00
P1
P2
D+
D−
PC
100

Fig.2

Fig.3

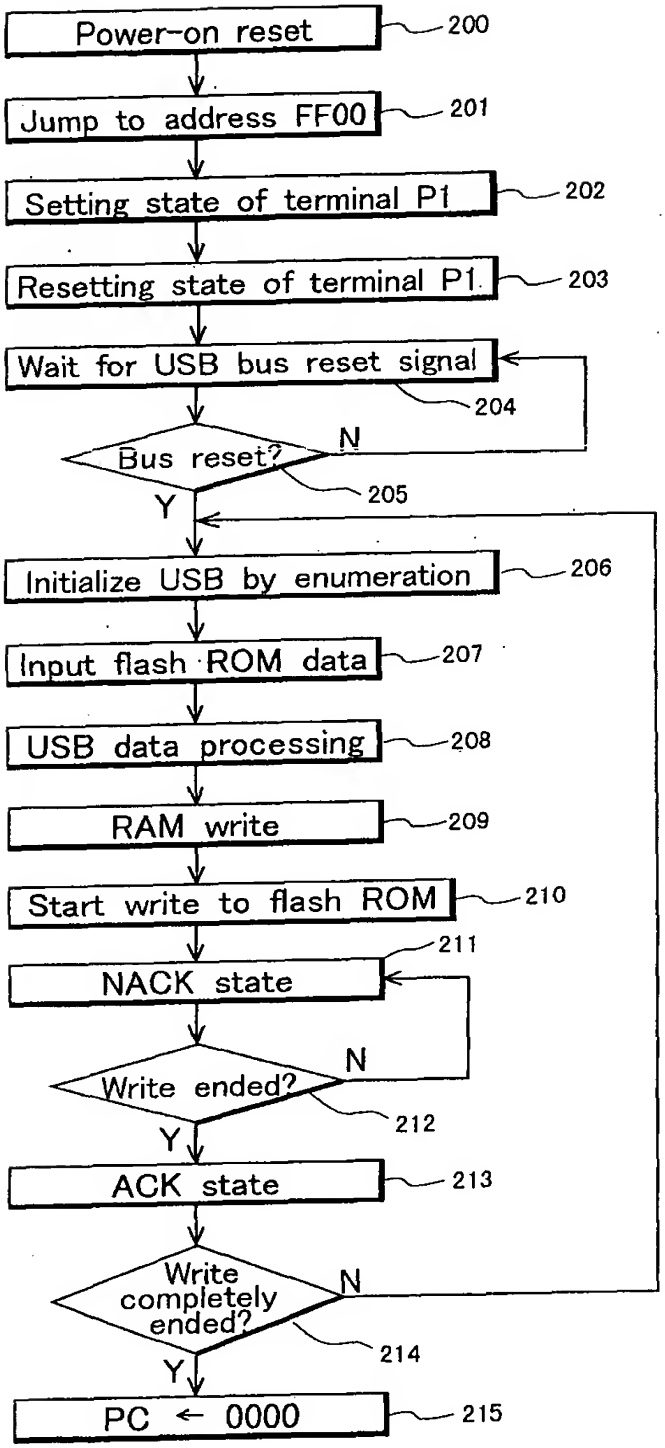
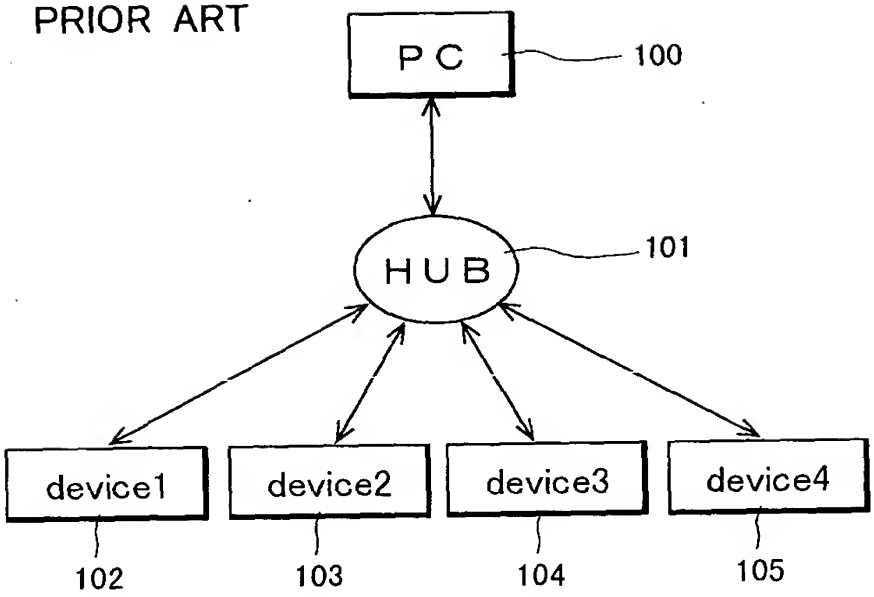

Power-on reset
200
Jump to address FF00
201
Setting state of terminal P1
202
Resetting state of terminal P1
203
Wait for USB bus reset signal
204
Bus reset?
N
205
Y
Initialize USB by enumeration
206
Input flash ROM data
207
USB data processing
208
RAM write
209
Start write to flash ROM
210
NACK state
211
Write ended?
N
212
Y
ACK state
213
Write completely ended?
N
214
Y
PC ← 0000
215

Fig.4

PRIOR ART